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(54) TESTING DIGITAL SIGNAL LINKS

(71) We, Hewlett Packard Limited, a British Company, of South Queensferry, West Lothian, Scotland, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to apparatus and a method of testing digital signal links. The invention relates more particularly to testing circuitry, such circuitry may, for example measure error rates and synchronisation loss rates on digital data links, such as are used for example for the transmission of pulse-code modulated (PCM) signals, by injecting into the data link a digital test signal having accurately known characteristics and then analysing the resultant received signal for the desired error information.

Digital data links must be assessed according to different standards that commonly find no counterpart in analogue or continuous-wave transmission systems. Of particular importance in digital data links are such factors as statistical errors in the received binary signal and the rate of loss of synchronization.

According to the invention, digital signal apparatus comprises first means including a plural number of logic elements, each of said logic elements having an input and an output and being operable to produce a signal at said output a selected time interval after the application of a signal to said input; and including coupling means coupling the output of one of the logic elements of the first means to the input of another logic element of the first means for forming a primary signal circuit of cascaded logic elements and for providing at least one auxiliary signal input between a pair of said plural number of logic elements; a signal input; at least one auxiliary signal circuit coupled to an auxiliary signal input and to the input of a logic element which precedes the auxiliary signal input in the cascaded logic elements of the primary signal circuit of the first means; said auxiliary signal circuit being operable to apply to the auxiliary signal input and to the input of said one logic element a selected one of either a signal present at said signal input for operation through a sequence of logic states in response to signals at said signal input or a signal present at the output of a logic element which succeeds the auxiliary signal input in the cascaded logic elements of the primary signal circuit for recurring operation through a sequence of logic states.

The invention also provides, in digital signal apparatus including a plurality of cascaded logic elements forming a shift register stage which has an output and which has a signal port coupled to an input of the cascade arrangement and to an auxiliary input intermediate a pair of logic elements in the cascade arrangement and which operates through a selected sequence of digital signals in response to signals applied to the signal port from the output of the cascade arrangement, the method of selectively synchronizing the operation of the cascade arrangement of logic elements to the operation of a source which produces digital signals in said selected sequence comprising the steps of: connecting the signal port to receive the digital signals from the source to alter the signal appearing at the output of the cascade arrangement; comparing the digital signal received from the source with the signal at the output of the cascade arrangement for determining the establishment of a predetermined relationship between the sequences thereof; and altering the connection of the signal port to receive the output of the cascade arrangement in response to establishment of said predetermined relationship for operating the cascade arrangement of logic elements through said selected sequence in synchronism with operation of the source through the same selected sequence.

The invention will now be particularly described with reference to the accompanying drawings, in which:—

Figure 1 is a block diagram showing the

present test circuitry coupled to a digital data link;

Figure 2 is a block diagram of another embodiment of the present test circuitry which includes apparatus for detecting error rate and synchronization loss rate;

Figure 3 is a block diagram of a multiple-return, shift-register generator;

Figure 4 is a block diagram of a shift register word circulator;

Figure 5 is a block diagram of combined feedback and feed-forward shift-registers according to the present invention;

Figure 6 is a chart showing the synchronizing operation of the circuitry of Figure 5;

Figure 7 is a block diagram of the error detecting and re-synchronizing circuitry of the present invention; and

Figure 8 is a block diagram of the synchronization loss detection circuitry of the present invention.

Referring now to Figure 1, there is shown a general arrangement of the presently preferred test circuitry and a data link under test. A digital signal from a signal source such as a telephone encoder, teleprinter, or computer, is normally fed to the input 9 of suitable interfacing circuitry 11 and then to a transmission line or cable. The interface circuitry 11 may provide coding for error detection-correction purposes, insertion of synchronizing words, time division multiplexing, or the like, but these are features of the particular system rather than of digital data links generally.

The data channel 13 may contain repeaters (typically, PCM telephone links operating, for example, on 1.536 MHz in Great Britain and 1.544 MHz in the United States of America and have repeaters located every 2000 yards). Such repeaters may have internal clock oscillators which are locked on to the incoming data bit rate. If the incoming data contains a long string of identical digits, the clock oscillator free-runs slightly fast or slow. In this case, a bit of information may be gained or lost and thus synchronism of the system may be lost.

At the receiving end of the channel 13, interfacing equipment 15 performs the opposite function of converting the received data into the form in which it was originally generated. Since there is always noise present at the receiving end of such a link, any threshold detector used to distinguish the various levels of the digital signal is subject to errors.

To test such data links as these, it is often necessary to use a digital signal having well-defined characteristics and a definite pattern which can be generated both at the transmitting end, and again at the receiving end. The locally generated pattern can then be compared with the received pattern, and errors in the received pattern can be analysed. A suitable pattern for a digital test signal may be a circulating word (e.g. 110100 110100 110100) or a pseudo-random binary sequence, but must be such that knowledge of a few digits enables the next digits to be uniquely determined. For example, in the above example, if the sequence 110100 is received, then without doubt the next digit should be 1.

Referring now to Figure 2, the digital test sequence is produced in synchronism with a clock 17 using a shift register generator (S.R.G.) 19 which can either be set up to generate a pseudo-random binary sequence or to circulate a predetermined word which is repeated indefinitely. Shift register generators of this type are described in the literature (see, for example, the Hewlett-Packard Journal, September 1967, and "The Theory of Autonomous Linear Sequential Networks" by B. Elspas, Trans. I.R.E. Circuit Theory, March 1959). Thus, the binary output of the generator is fed to the data link via a suitable interfacing unit 11 and at the receiving end is converted back into a form suitable for the logic circuitry used in the receiver by the input interface 15.

The receiver contains a generator 21 similar to that used in the transmitter but with an additional capability that upon a command signal applied to it via line 23 the digital signal generated thereby can be resynchronized on the received data in a very few clock periods. Normally, this command signal is "off" and the receiver generates an identical sequence, of digits to that received at the input interface 15 but with no errors. The local generator 21 may be triggered by a clock extraction circuit 22 at the line/receiver interface 15 which generates a clock signal from the received signal if such a clock signal is not available at the receiver end of the line. The output sequence from the receiver generator 21 is then compared in comparator 25 with the received sequence so that the errors in the received sequence can be detected and fed to classification and display circuitry 27.

The error information from comparator 25 is also fed to a second shift register in synchronization-loss detector 29 which analyses the form of the error stream in order to distinguish between the ordered error pattern which results from a loss of synchronization and the error stream generated by other faults of the system. These latter errors may be random or correlated, but the nature of the circuitry, as described later herein, enables the exact form of the error pattern due to synchronization loss to be distinguished from any other error pattern that may arise. Thus, when detector 29 detects a loss of synchronization, it supplies a command signal to the receiver generator 21 via line 23 to

enable the generator 21 to resynchronize with the received signal.

Additional circuits at the receiver end may include a violation detector 31 which enables violations of the format rules to be detected (e.g. for a bipolar or Pair Selected Ternay signal as described in "An Experimental 224 Mbit/sec repeatered line", B.S.T.J., September 1966, p. 933, certain sequences of +,0,− pulses are not generated by the transmitter output interface but will generally appear at the receiver input when errors are present). Also, gating circuits (not shown) may be included in the receiver to prevent the display of error information when the error results from loss of synchronization and such loss of synchronization has been detected or is being corrected.

Referring now to Figure 3, there is shown a simplified form of the shift register generators used in the system of the present invention. Typically the shift register comprises a plurality of flip-flops 33—41 whose initial states may be programmed. Each flip-flop is coupled to receive clock pulses on one input and is also coupled through a programmable exclusive-OR gate 43—47 to receive on another input either the output of the preceding flip-flop or the modulo-2 sum of (i.e., output of the exclusive-OR gate of which the inputs are) the output of the preceding flip-flop and the output which is fed back from the last flip-flop 41 so that, in effect, the shift register may be connected according to any selected format by operating the programming switches. For simple fixed word circulation, the flip-flops may be set in selected initial states and the feedback inputs and the interstage gates may be disabled, as shown in Figure 4, to provide a shift register word generator. (Clock pulse inputs are conventional and have been omitted for simplicity). Also, a shift register generator similar to the one shown in Figure 3 having feedback from the output of the last stage 49 to selected inputs (via interstage gates) may be connected to another shift register having identically positioned interstage gates which are connected to receive feed-forward signals from the input of the first stage 51, as shown in Figure 5. In this configuration, it can be shown that after 6 clock pulses the contents of the shift register 50 second in line will be identical to the contents of the shift register 48 first in line. If this condition is not initially so, then for N-stage registers, not more than N clock pulses, applied simultaneously and at the same rates to the registers, will be required to synchronise the two registers. As an example, consider that the first-in-line register 48 has the initial contents 010011 and that the second-in-line register 50 has the initial contents 111001. Then, as shown in Figure 6, after 6 shift (or clock) pulses the contents of the two registers are identical and remain so thereafter. This aspect enables synchronization losses to be distinguished conveniently from error bursts by the synchronization-loss detector described later herein, and also enables resynchronization of the local generator following the detection of a loss of synchronism as follows:—

Errors are detected by comparing the output signal of the local receiver generator with the received signal from the transmitter. Figure 7 shows a 4-stage example of an error detecting system in which the local receiver generator 53 is switchable to be either a feed-forward or a feedback shift register as required. With the switch 55 in position 2, the second (receiver) shift register 53 acts as an identical generator to that in the transmitter, and their outputs are compared to produce the desired error information at the output of the non-equivalence gate 57 that is connected to receive the outputs of the transmitter and receiver shift registers 52 and 53. With the switch 55 in the position 1, the resynchronising process described in connection with Figure 5 will take place so that the receiver synchronizes with the received data provided that N bits of data (where N=4 in Figure 7, N=6 in Figure 5) are received consecutively without intervening errors.

If the received sequence and the locally-generated sequence lose synchronism with one another, then the error pattern thus produced will be a periodic sequence. This sequence will be the same as the locally generated sequence, or in the case of non-maximal generators will be one of the sequences which can be generated by the local or transmitter generators in the configuration in which they are being used. That is, for word circulation and for pseudo-random binary sequences of non-maximal or maximal period, the error sequence is a shift-and-add sum of the original sequence.

The shift-and-add properties of maximal-length sequences are well known and are described in the literature (see, for example, "Introduction to Linear Shift-Register Generated Sequences", University of Michigan Research Institute, Technical Report No. 90, October 1958, A.D. No. 281272). For any shift other than zero, the new sequence produced is identical to the original sequence but is shifted with respect to both of them, and for zero shift, the modulo-2 sum is aways zero.

For non-maximal sequences, a new sequence is generally produced by the shift-and-add process, but this new sequence is always one of the other sequences generated by the same shift register generator. The length of the new sequence is always the same as, or is a factor of the length of, the original sequence. For example, the 6-bit

sequence 110011 generated by a 4-stage shift register generator having feedback to the first and third stages gives rise to the following sequences:

(a new 6-bit sequence)	1 bit shift	001010
(6-bit sequence identical to original)	2 bit shift	001111
(a new 3-bit sequence)	3 bit shift	101101
(6-bit sequence identical to original)	4 bit shift	111100
(a new 6-bit sequence identical to sequence generated by 1 bit shift).	5 bit shift	010100

Each of these sequences repeats every 6 bits (sometimes less, but never more) and thus can be used at the input to the feed-forward register 59 at the receiver end for the detection of loss of synchronization.

For word circulation, this is merely a particular case of non-maximal sequence generation, and the shift-and-add properties are identical to those for non-maximal sequence generation.

In a maximal or a non-maximal generator (and in a word circulator which is only a special case of the latter) then if the error sequence is due to a synchronization-loss and is thus a shift-and-add sum, it can be recognised by an additional feed-forward shift register 59, as shown in Figure 8, the output to which is the output of the error detector (in tha binary case, the comparator is merely a modulo-2 adder; systems having other moduli can be accommodated using other types of linear comparison circuits which take the modulo-n difference between the two inputs rather than the sum. In modulo-2, the sum and difference are identical functions. For further information on feedback shift register generators using higher moduli than 2, see B. Elspas, op. cit.).

In Figure 8, the synchronization-loss detecting shift register 59 is connected to recognise the sequence of errors caused by a loss of synchronisation. The error line 71 contains the shift-and-add sum of the outputs of the two generators 61, 63 which is the error sequence caused by the loss of synchronization. The feed-forward shift register 59 "locks" onto the error sequence as though it were generated by a single generator having the same structure as one of the two shift registers 61, 63 of Figure 8. Thus, after N clock periods from the time of the synchronization loss, the last stage of the synchronization-loss detector shift register 59 contains the same bit (0 or 1) as the input terminal 71, since this terminal carries the last bit of the hypothetical single generator formed by the two shift registers 61, 63. Thus, by comparing the input and the output of the synchronization-loss detector 59 in gate 65, an indication of a synchronization-loss having occurred is obtained at gate output 67.

An OR gate 69, as shown dotted in Figure 8, is provided to distinguish between the following operating conditions:

When the shift register generators 61 and 63 are synchronized, output 71 of the error detector is a string of zeros, and thus the signal A) at output 67 will also be a zero whenever the system is synchronized. However, this case can be distinguished from the synchronization-loss case by the fact that when a synchronization-loss has occurred, there is always at least one stage in the synchronization-loss detector shift register 59 containing a logic "1". Thus, OR gate 69 connected to each of the stages of the shift register 59 produces an output "1" at terminal 73 (signal B) when a synchronization-loss has occurred. Thus, the states in which the synchronization-loss detector 59, 65, 69, etc. can exist are as follows:

1) In synchronization; no errors
A=0 always
B=0 always

2) In synchronization; errors present
A=is indeterminate for N bits following each error; thereafter A=0
B=1 for up to N bits following the error

3) Out of synchronization; no errors
A=0 after the 1st N bits of lost synchronization, and subsequently always 0
A=is indeterminate during the 1st N periods following the synchronization-loss
B=1 always

4) Out of synchronization; errors present
A and B are indetermine, but if 2N consecutive correct bits are received, the logical process to be described will correctly distinguish the loss of synchronisation.

This logical process is as follows:

A and B are fed to an AND gate 75 which enables gate 77 to permit counter 79 to count clock periods when the output of AND gate 74 is a logic 1. This corresponds to case 3) above. If either A becomes a logic "1" or B becomes a logic "0", the counter 79 is reset to zero. If the counter 79 reaches a count of N (the minimum number of periods necessary to ensure that the conditions set up are due to a loss of synchronization) then a command signal is sent via line 23 (81) to the receiver generator 63 to convert it to a feed-forward shift register, as

shown in Figure 7. Shift register 63 is held in this configuration for N clock periods after which the counter 79 is reset and the synchronization-loss detecting shift register 59 is reset to zero. This period enables the shift register to resynchronize on the received data provided the data is correct.

Thus, the synchronization-loss detection and resynchronization process takes 3N clock periods to perform (N periods to set up the synchronization-loss detecting shift register 59; N periods to ensure that the subsequent conditions are due to a synchronization-loss, and N periods to resynchronize) rather than about 2^N periods typically required for a systematic search through a maximal length sequence. In practice, for a 30-stage maximal shift register running at 100 MHz, the detection and resynchronization process of the present invention takes less than one microsecond rather than the 10 second sequence length for a conventional systematic search.

Note that throughout this paper, the use of the so-called multiple return generator as described by B. Elspas (op cit.) has been made. The principles involved work equally well with simple generators of the type described by Birdsall and Ristenbatt (op cit.) but Multiple generators have certain advantages of speed and programmability not possessed by simple generators. To every multiple return generator there is a corresponding simple generator which produces identical sequences and vice versa.

WHAT WE CLAIM IS:—

1. Digital signal apparatus comprising:

first means including a plural number of logic elements, each of said logic elements having an input and an output and being operable to produce a signal at said output a selected time interval after the application of a signal to said input; and including

coupling means coupling the output of one of the logic elements of the first means to the input of another logic element of the first means for forming a primary signal circuit of cascaded logic elements and for providing at least one auxiliary signal input between a pair of said plural number of logic elements;

a signal input;

at least one auxiliary signal circuit coupled to an auxiliary signal input and to the input of a logic element which precedes the auxiliary signal input in the cascaded logic elements of the primary signal circuit of the first means; said auxiliary signal circuit being operable to apply to the auxiliary signal input and to the input of said one logic element a selected one of either a signal present at said signal input for operation through a sequence of logic states in response to signals at said signal input or a signal present at the output of a logic element which succeeds the auxiliary signal input in the cascaded logic elements of the primary signal circuit for recurring operation through a sequence of logic states.

2. Digital signal apparatus according to claim 1 comprising also

second means including said plural number of logic elements, each having an input and an output and being operable to produce a signal at said output a selected time interval after the application of a signal to said input;

coupling means for said second means coupling the output of at least one logic element of the second means to the input of at least another logic element of the second means for operating recurringly through a sequence of logic states which is similar to a sequence of logic states produced during recurring-sequence operation of the first means; and

circuit means including a digital signalling circuit for applying the recurring sequence of logic states from the second means to the signal input of the first means.

3. Digital signal apparatus according to claim 2 comprising:

control means coupled to said signal input and to the output of said logic element which succeeds the auxiliary signal input of the first means for controlling the selection of the signal at said signal input for synchronizing the operation of the logic elements of the first and second means through a sequence of logic states, and the output signal of the first means for providing an indication of error in the transmission of a sequence of logic states from the second means to the first means through said digital signalling circuit.

4. Digital signal apparatus according to claim 1 comprising also

gate means coupled to receive the signal at said signal input and the signal at said output of a logic element of the first means for producing an error output signal as the combination of such signals;

additional means including a plural number of logic elements, each of said logic elements having an input and an output and being operable to produce a signal at said output a selected time interval after the application of a signal to said input;

coupling means coupling the output of one of the logic elements of said additional means to the input of another logic element of said additional means for forming a primary signal circuit of cascaded logic elements and for providing at least one auxiliary signal input between a pair of said plural number of logic elements of said additional means, the arrangement of logic elements and auxiliary signal inputs in said first and additional means being substantially similar;

At least one auxiliary signal circuit coup-

led to an auxiliary signal input and to the input of a logic element which procedes the auxiliary signal input in the cascaded logic elements of the primary signal circuit of said additional means, and operable to apply signals on said auxiliary signal circuit to the input of said one logic element and to said auxiliary signal input;

means coupled to the auxiliary signal circuit of said additional means for applying thereto said error output signal from the gate means; and

control input means coupled to an output of a logic element of said additional means succeeding said auxiliary signal input in the primary signal circuit of said additional means, and coupled to receive said error output signal for controlling the selection in the first means of either the signal present at said signal input or said signal present at the output of said logic element of the first means which succeeds said auxiliary signal input.

5. Digital signal apparatus according to claim 4 wherein said control input means also includes

a first gate coupled to receive signals at the outputs of the logic elements of said additional means for producing a first reference output signal as a logic combination of such outputs;

a second gate coupled to receive the output of a logic element of said additional means succeeding said auxiliary signal input in the primary signal circuit of the additional means, and coupled to receive said error output signal for producing a second reference output signal; and

a synchronizing circuit responsive to the recurrence of a logic combination of the first and second reference output signals a number of times greater than said plural number of logic elements of said first means for operating said auxiliary signal circuit of the first means to receive signal present at said signal input for synchronizing the operation of the logic elements of the first means through a sequence of logic states with a sequence of logic states appearing on said signal input.

6. Digital signal apparatus substantially as hereinbefore described with reference to and as illustrated in figures 2 to 8 of the accompanying drawings.

7. In digital signal apparatus including a plurality of cascaded logic elements forming a shift register stage which has an output and which has a signal port coupled to an input of the cascade arrangement and to an auxiliary input intermediate a pair of logic elements in the cascade arrangement and which operates through a selected sequence of digital signals in response to signals applied to the signal port from the output of the cascade arrangement, the method of selectively synchronizing the operation of the cascade arrangement of logic elements to the operation of a source which produces digital signals in said selected sequence comprising the steps of:

connecting the signal port to receive the digital signals from the source to alter the signal appearing at the output of the cascade arrangement;

comparing the digital signal received from the source with the signal at the output of the cascade arrangement for determining the establishment of a predetermined relationship between the sequences thereof; and

altering the connection of the signal port to receive the output of the cascade arrangement in response to establishment of said predetermined relationship for operating the cascade arrangement of logic elements through said selected sequence in synchronism with operation of the source through the same selected sequence.

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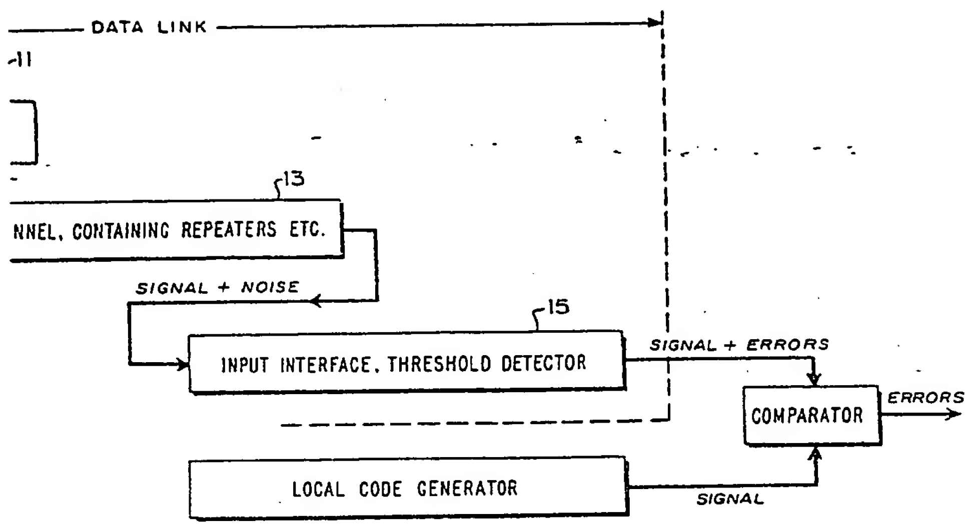
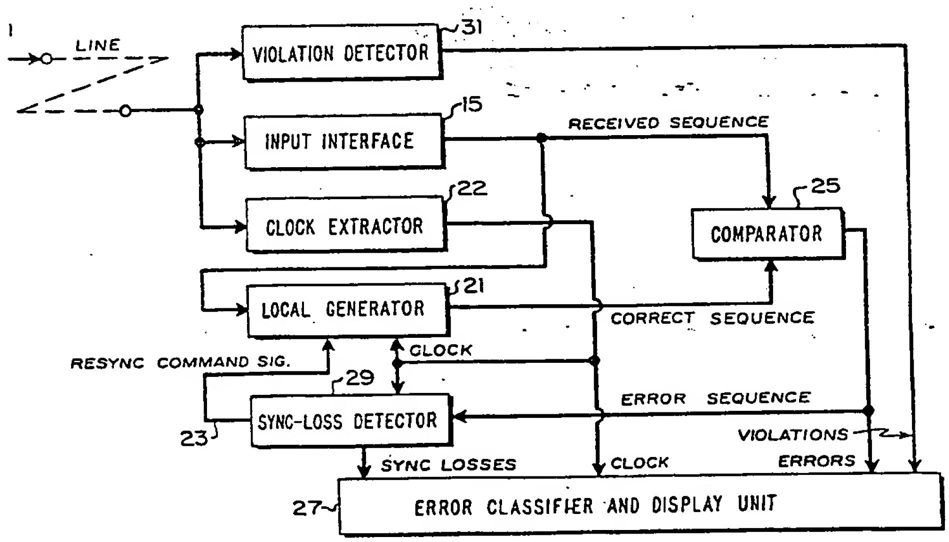
1261749 COMPLETE SPECIFICATION
5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1





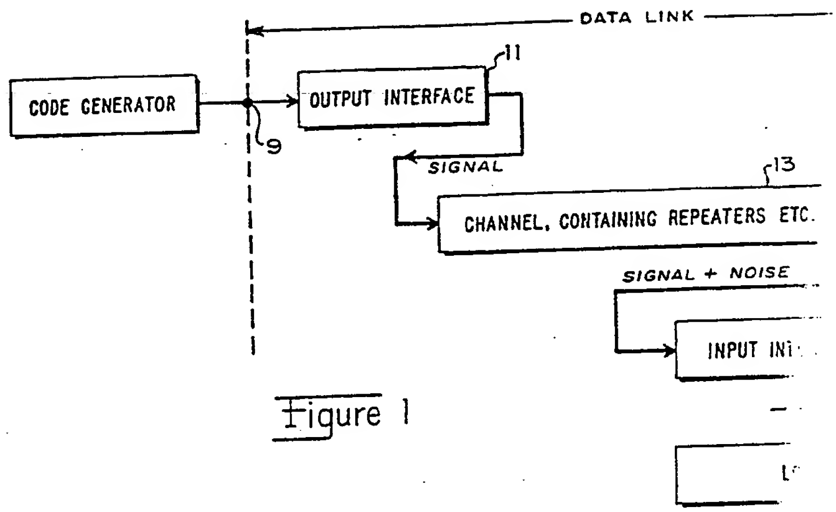


Figure 1

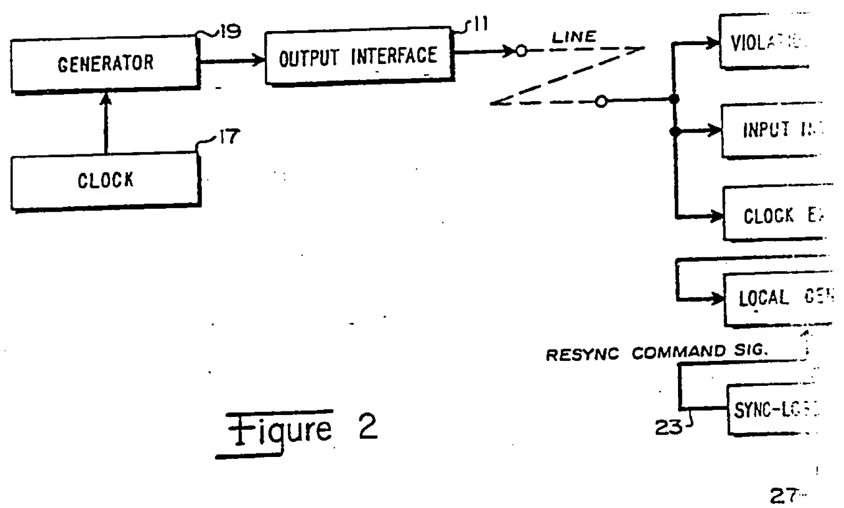


Figure 2

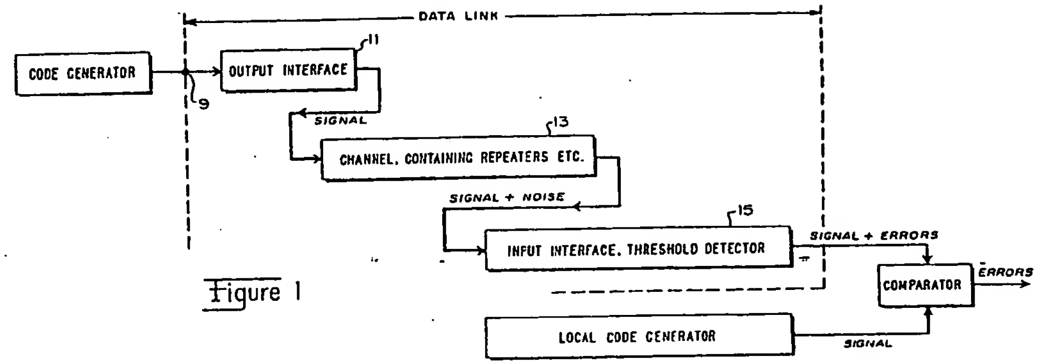


Figure 1

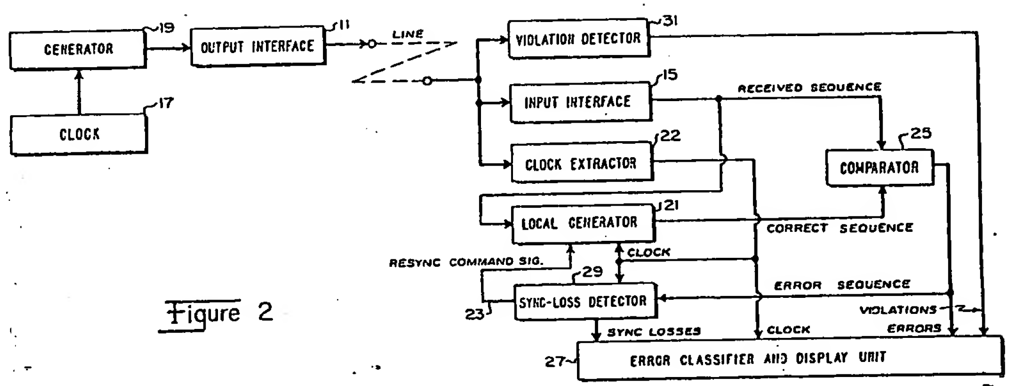
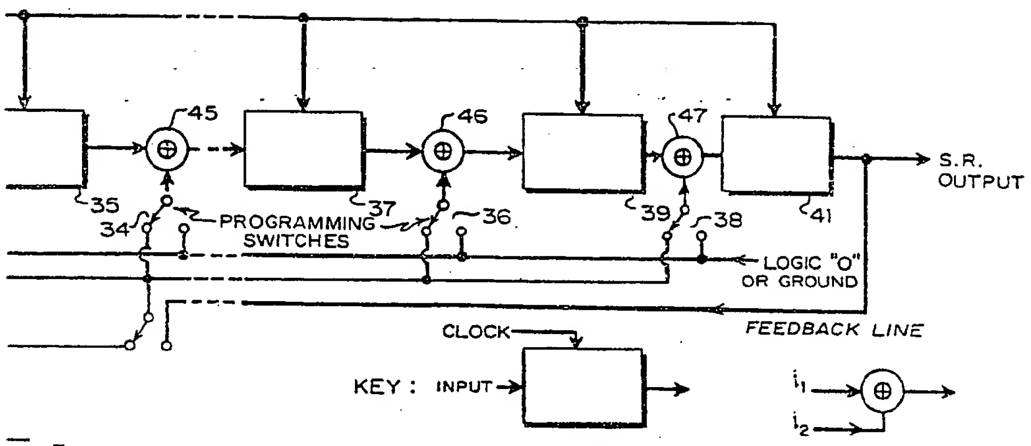


Figure 2



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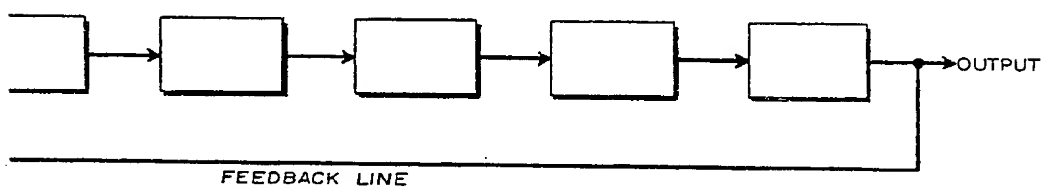


Figure 4

Word Circulator

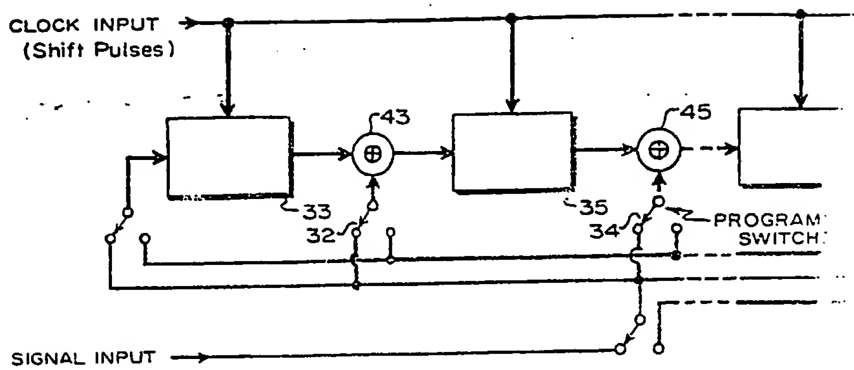
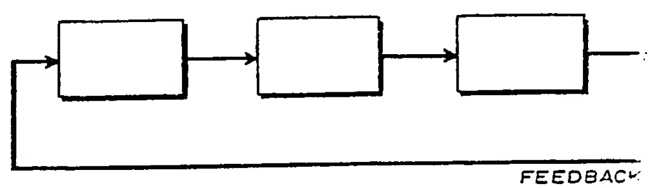


Figure 3

Programmable Multiple Return Shift Register



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Word Circ

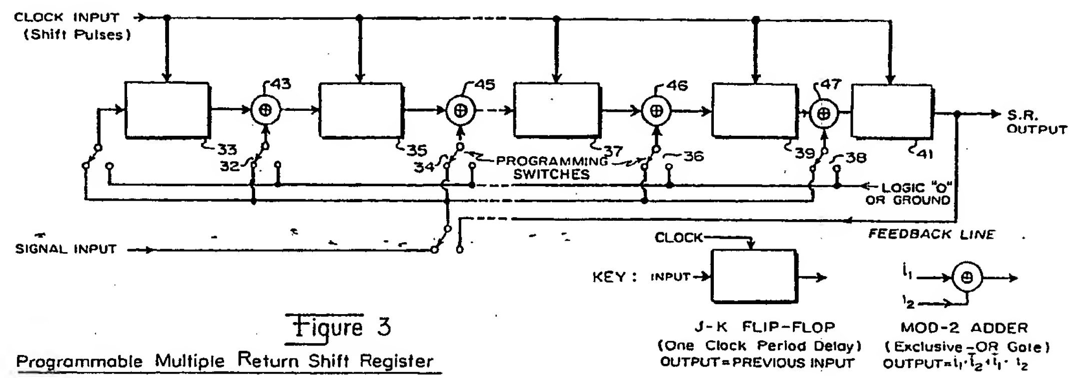

Figure 3
Programmable Multiple Return Shift Register

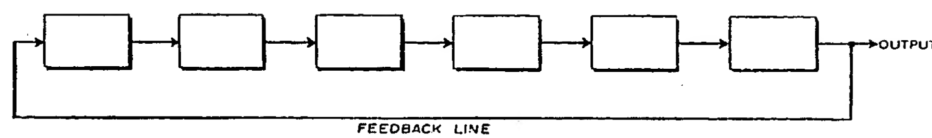

Figure 4
Word Circulator

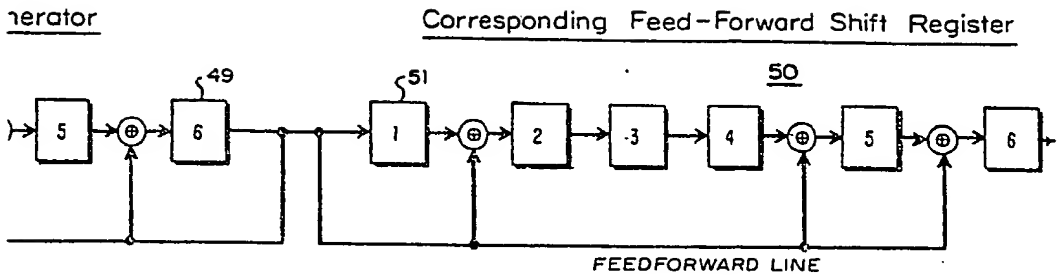

Figure 5

Vectors of The S.R.'s Shown Above

	5	6
	1	1
	1	0
	0	1
	0	1
	0	1
	0	1
	0	1
	1	1
	1	0
	0	1
0	1	1

RIGHT

1	2	3	4	5	6
1	1	1	0	0	1
1	0	1	1	1	1
0	1	0	1	1	1
1	1	1	0	0	0
1	0	1	1	1	1
1	0	0	1	0	0
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	0	1	0
0	1	0	0	0	1
1	1	1	0	1	1

ETC

CORRECT BITS BELOW AND LEFT OF STAIRCASE

INCORRECT BITS

CONTENTS IDENTICAL

IN SYNC FROM HERE ON

Figure 6

Shift Register Generator

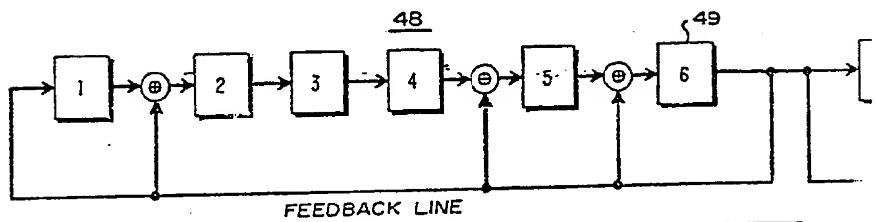

Figure 5

Content Vectors of The S.R.'s

LEFT

STAGE NUMBER → / CLOCK PERIODS ↓	1	2	3	4	5	6
0	0	1	0	0	1	1
1	1	1	1	0	1	0
2	0	1	1	1	0	1
3	1	1	1	1	0	1
4	1	0	1	1	0	1
5	1	0	0	1	0	1
6	1	0	0	0	0	1
7	1	0	0	0	1	1
8	1	0	0	0	1	0
9	0	1	0	0	0	1
10	1	1	1	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮
ETC			ETC			

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Figur

Shift Register Generator | Corresponding Feed-Forward Shift Register

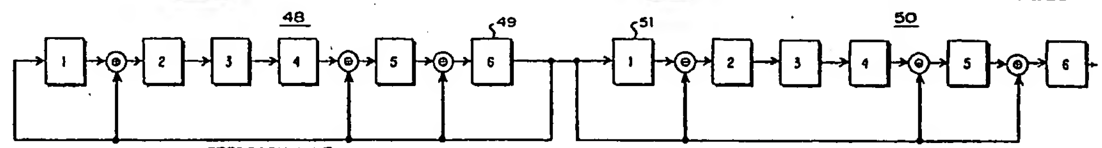


Figure 5

Content Vectors of The S.R.'s Shown Above

LEFT

CLOCK PERIODS \ STAGE NUMBER →	1	2	3	4	5	6
0	0	1	0	0	1	1
1	1	1	1	0	1	0
2	0	1	1	1	0	1
3	1	1	1	1	0	1
4	1	0	1	1	0	1
5	1	0	0	1	0	1
6	1	0	0	0	0	1
7	1	0	0	0	1	1
8	1	0	0	0	1	0
9	0	1	0	0	0	1
10	1	1	1	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮
ETC		ETC				

RIGHT

1	2	3	4	5	6
1	1	1	0	0	1
1	0	1	1	1	1
0	1	0	1	1	1
1	1	1	0	0	0
1	0	1	1	1	1
1	0	0	1	0	0
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	0	1	0
0	1	0	0	0	1
1	1	1	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮
		ETC			

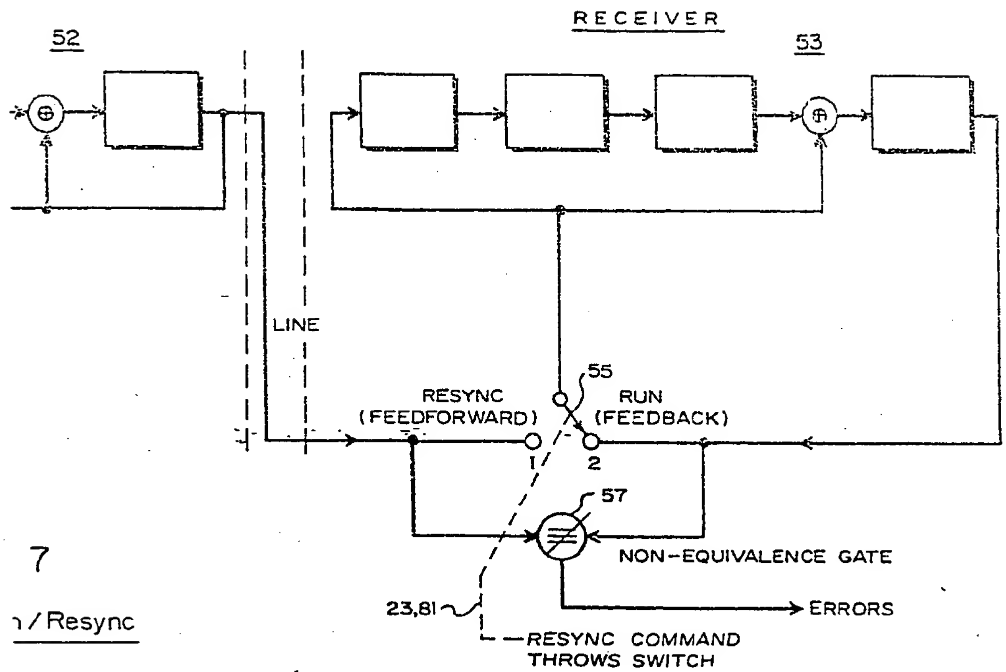
CORRECT BITS BELOW AND LEFT OF STAIRCASE

INCORRECT BITS

CONTENTS IDENTICAL

IN SYNC FROM HERE ON

Figure 6


RECEIVER
52
53
LINE
55
RESYNC
(FEEDFORWARD)
RUN
(FEEDBACK)
1
2
57
NON-EQUIVALENCE GATE
ERRORS
23,81
RESYNC COMMAND
THROWS SWITCH

7

ı / Resync

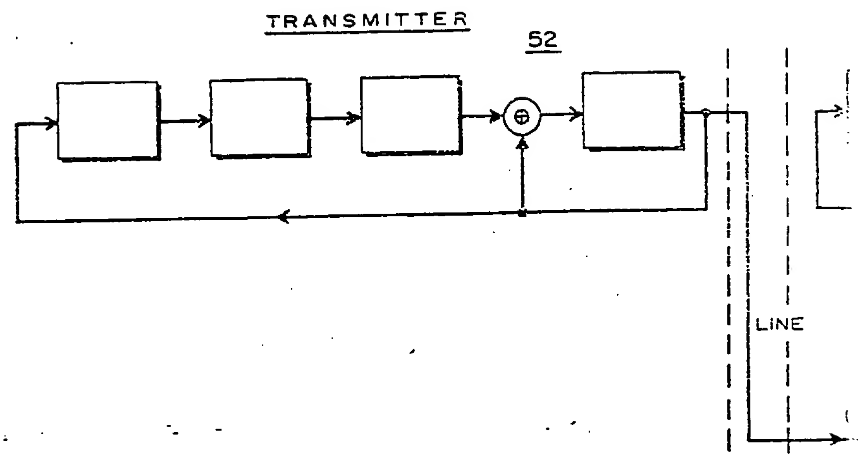


Figure 7
Error Detection / Resync

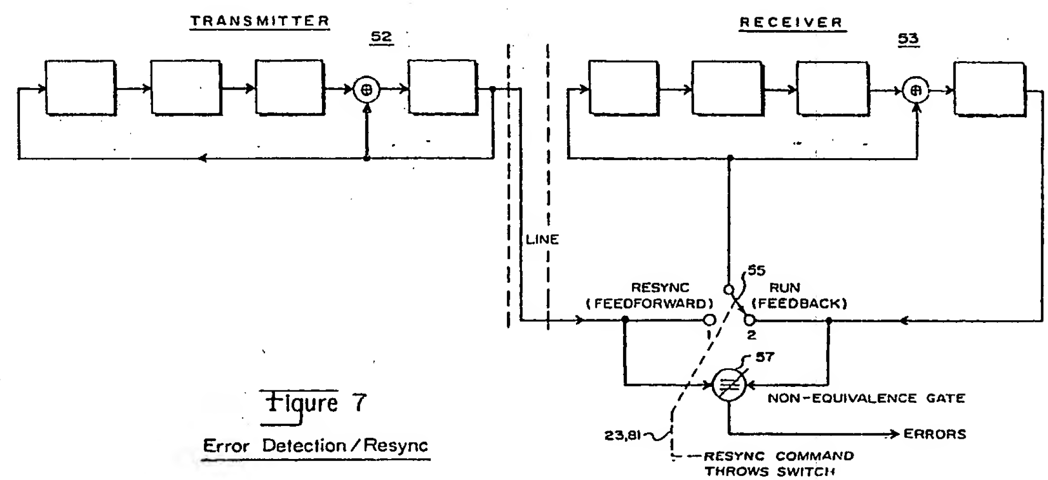


Figure 7
Error Detection / Resync

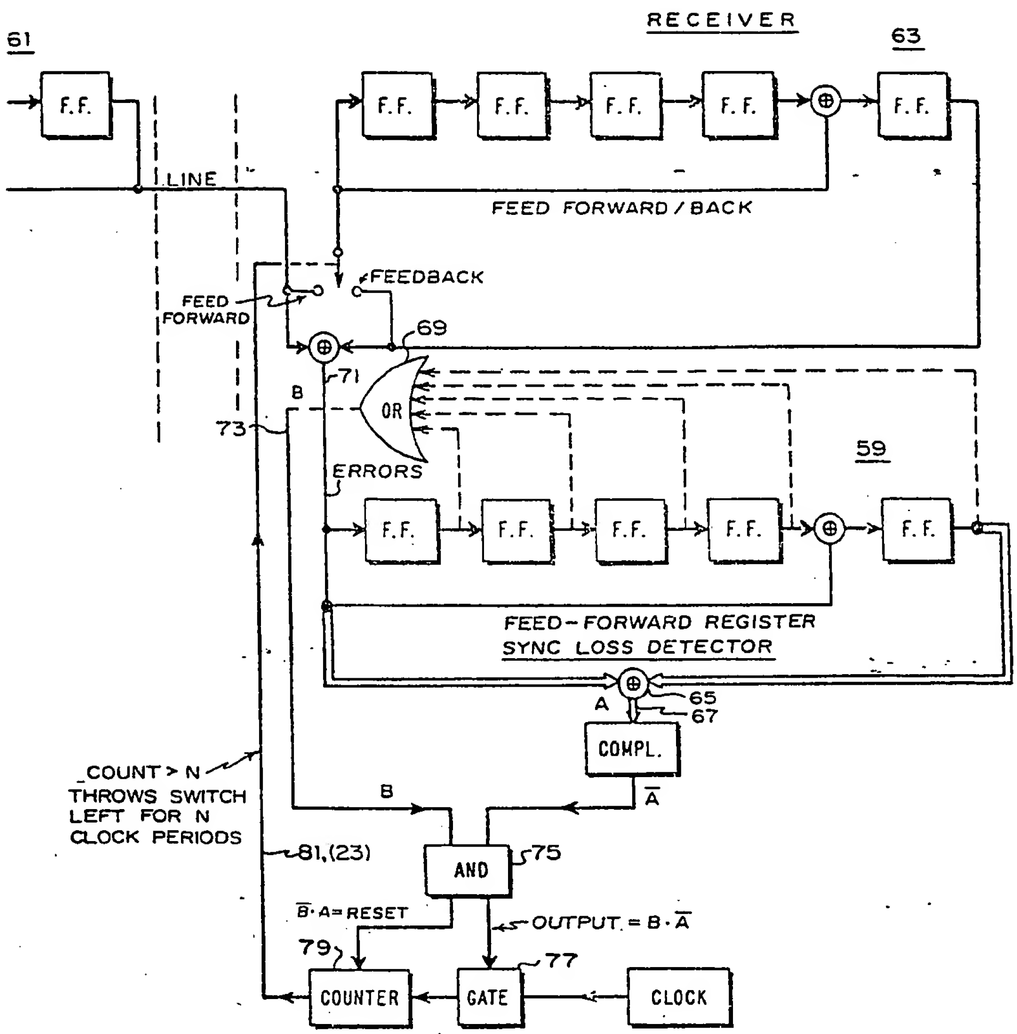

RECEIVER
61
63
F.F.
LINE
FEED FORWARD / BACK
FEEDBACK
FEED FORWARD
69
71
B
OR
73
ERRORS
59
FEED-FORWARD REGISTER
SYNC LOSS DETECTOR
65
67
A
COMPL.
COUNT > N THROWS SWITCH LEFT FOR N CLOCK PERIODS
B
$\overline{A}$
81,(23)
AND
75
$\overline{B}\cdot A$=RESET
OUTPUT = $B\cdot\overline{A}$
79
77
COUNTER
GATE
CLOCK

Figure 8

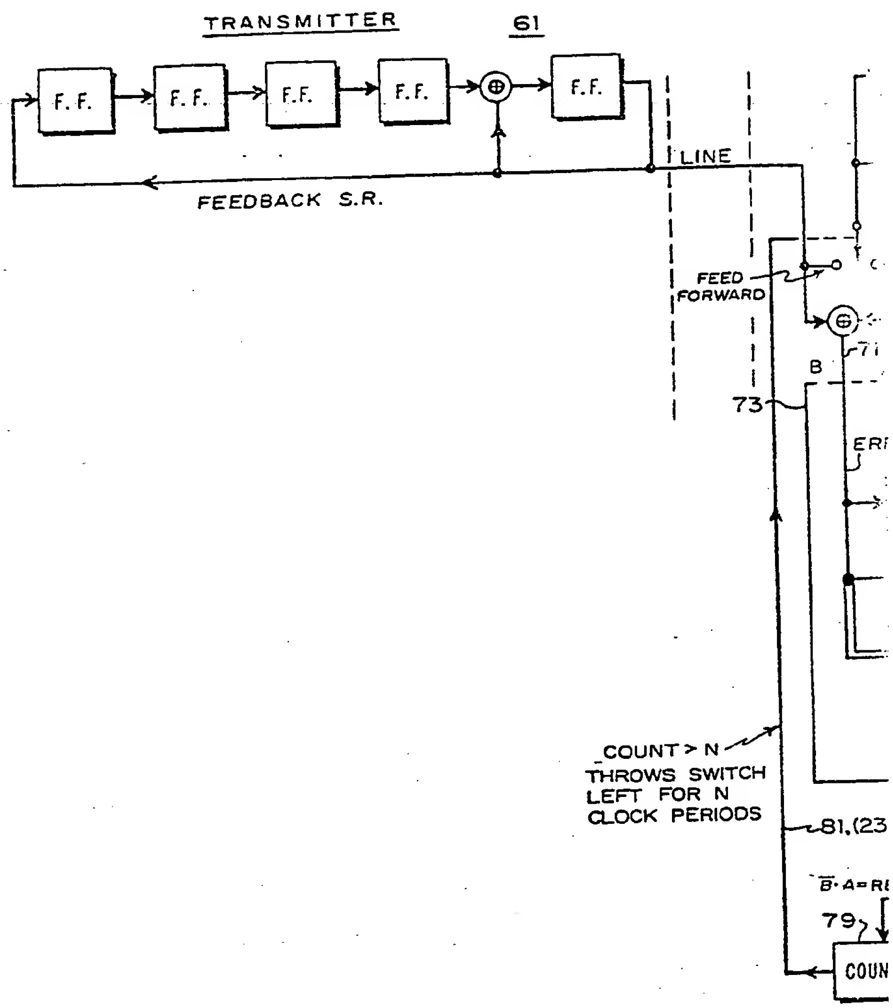

TRANSMITTER
61
F.F.
F.F.
F.F.
F.F.
F.F.
LINE
FEEDBACK S.R.
FEED FORWARD
71
B
73
ERI
COUNT > N THROWS SWITCH LEFT FOR N CLOCK PERIODS
81,(23
B̄·A=RE
79
COUN

Figure 8

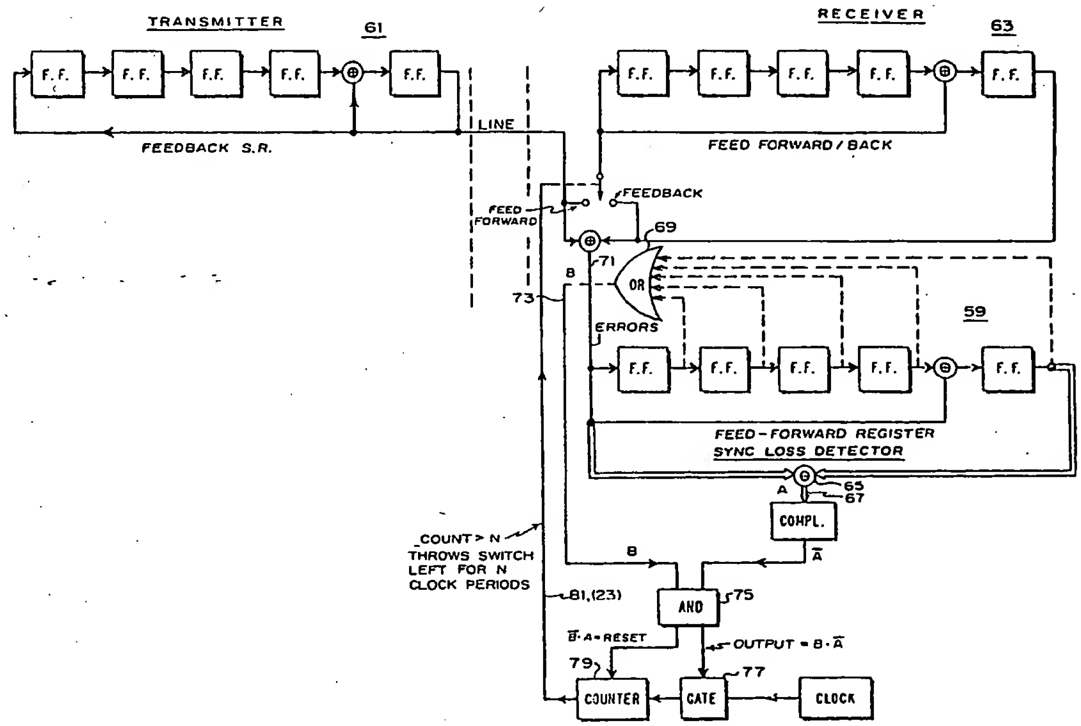

TRANSMITTER
61
F.F.
FEEDBACK S.R.
LINE
RECEIVER
63
FEED FORWARD / BACK
FEEDBACK
FEED FORWARD
69
71
OR
B
73
ERRORS
59
FEED-FORWARD REGISTER
SYNC LOSS DETECTOR
A
65
67
COMPL.
$\bar{A}$
COUNT > N THROWS SWITCH LEFT FOR N CLOCK PERIODS
B
81,(23)
AND
75
$\bar{B}\cdot A$ = RESET
OUTPUT = $B\cdot\bar{A}$
79
77
COUNTER
GATE
CLOCK

Figure 8